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2-6 GHz MONOLITHIC MICROWAVE AMPLIFIER

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ABSTRACT

The design and results of a GaAs monolithic feedback amplifier are presented. The features stressed are its small size (0.76 mm square) and simple 5 mask process in order that the lowest possible cost per dB of gain may be achieved. Refinements to the CAD model, particularly with respect to inductors, are also presented.

INTRODUCTION

The feedback amplifier using GaAs MESFETs was proposed by Ulrich (1), first made in hybrid form by Niclas (2), and recently fabricated in monolithic form by Terzian (3). It offers an excellent method whereby use of a series R-L network from drain to gate can simultaneously flatten the gain response and reduce the input and output VSWR. Niclas showed that the addition of inductance in the drain of the FET can be used to improve the high frequency response. All that has to be added to make a complete amplifier is biasing networks and a DC blocking capactior. Because of its simplicity, this amplifier configuration has the potential to be made as a very small monolithic device. Since cost per chip is proportional to the area of the chip, small size is emphasized to produce the lowest $/dB of broadband gain. The feedback configuration is not without drawbacks in terms of maximum frequency of operation and VSWR limitations. As a result, the frequency range chosen was the popular 2-6 GHz. band. Higher frequency of operation can be achieved if one improves the ratio of transconductance to gate capacitance of the FET, but that also increases processing complexity. This, in turn, can decrease yield and increase cost.

A completed device is shown in Figure 1 and the overall CAD model in Figure 2. Note that on-chip biasing of the drain is included. Since it was known that these devices would be cascaded, the location of the DC blocking capacitor was chosen so that the gate bias of one stage would be transferred to all the stages when joined by the RF wirebond between them. In this way, space on the chip could be reduced by not having separate gate biasing for each stage. In an amplifier consisting of several stages, the single gate bias connection would be via a quarter-wave wirebond from a chip capacitor near the monolithic devices.

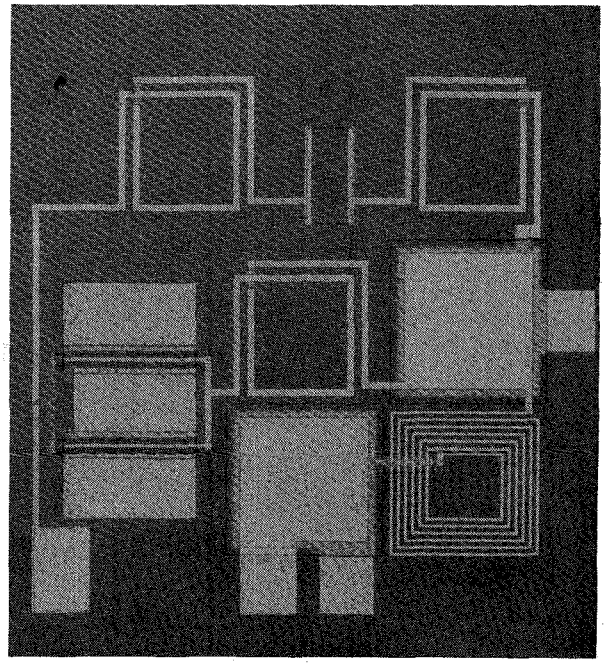

FIGURE 1 - Fabricated GaAs monolithic 2-6 GHz amplifier

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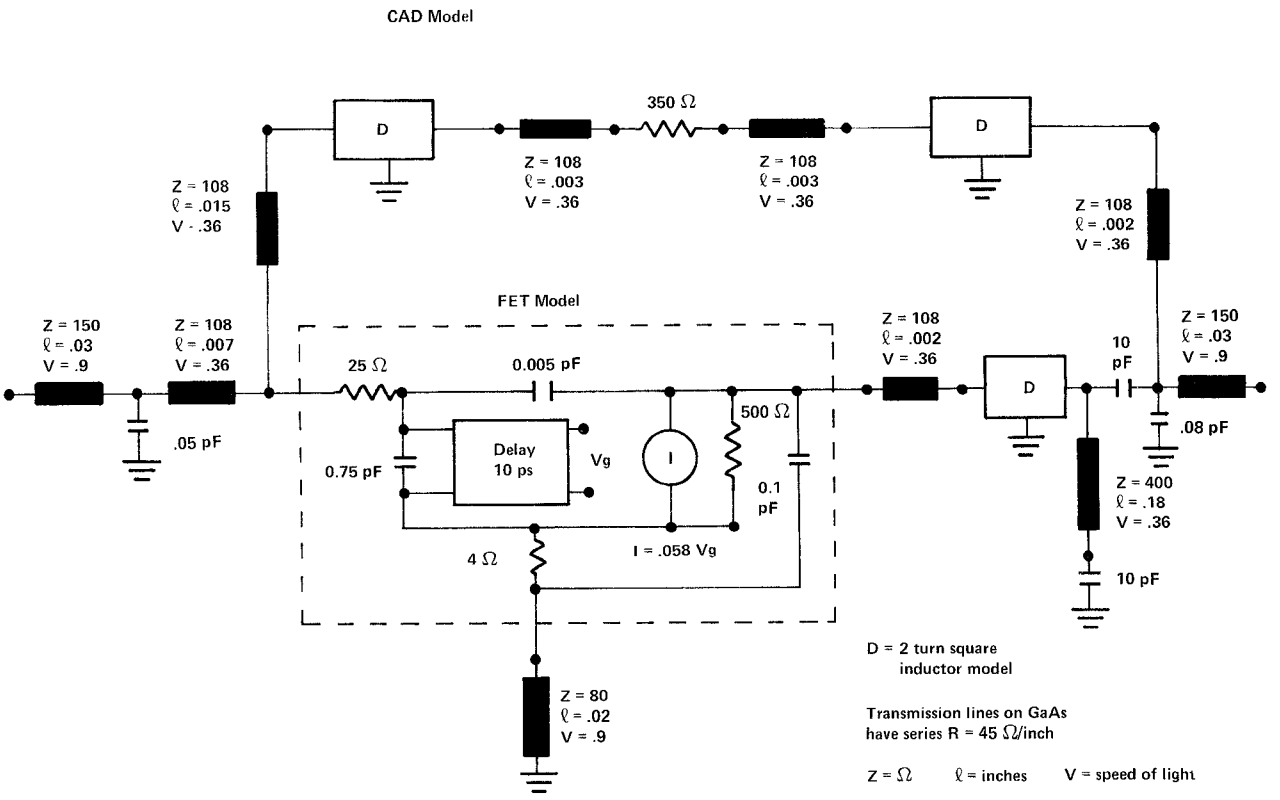

FIGURE 2 - CAD model of 2-6 GHz monolithic amplifier

PROCESS

Because the choice of process steps sets some constraints on the electrical design, these will be discussed first. A dominant driver in this project is low cost per unit of function (dB of gain, for instance). The goal has been to reduce the cost of amplifier gain from the range of $50/dB for present hybrid technology devices to the range of $5/dB for monolithic devices. Thus, the process sequence chosen was the simplest possible consistent with achieving useful results. The process, therefore, does not use electroplating, airbridges, or substrate via-connections for grounding, all of which are popular in the industry.

The masking sequence is as follows:

MASK 1, define the conducting areas for FETs and resistors by etching;

MASK 2, define by lift-off the AuGe- Ni-Au evaporated metallization for the source and drain of the FET, the ohmic contacts to the resistor, the bottom layer of the MIM capacitors and the underpasses;

MASK 3, define the dielectric areas used in the capacitors and the underpasses;

MASK 4, define by lift-off the Ti-Pt- Au metallization for the gate of the FET, the top of the MIM capacitors and the rest of the microwave circuit;

MASK 5, etch the resistor to its nominal value.

Both ion-implanted material (annealled in an As overpressure environment (4)) and chemical vapor deposited material has been successfully used. No gate notching is used, no n^+ layer is used, and the gate length is nominally 0.8 micron. All this is done in an effort to increase manufacturing and electrical yield. The dielectric is tantalum oxide (5), which is deposited using reactive RF magnetron sputtering. The edge coverage can be improved by applying a negative bias to the substrate electrode during sputtering. In its absence, a thin polyimide layer is used to prevent any edge shorts. The wafer is lapped and polished to 175 micron thickness, thick enough to reduce the chance of accidental breakage during later handling.

ELECTRICAL DESIGN

The electrical model in Figure 2 reflects the above process sequence. The FET parameters were determined by measuring previously processed wafers with only the FET and output inductor present, and fitting a model to the measured data. The most critical parameters are the transconductance, as it determines the overall gain, and the gate capacitance, as it determines the gain at the high end of the band. Because the gate capacitance is varied with the gate bias, it is predicted that the ±10% tolerance needed for proper circuit operation can be achieved 80-90% of the time. The drain-source resistance is often lower but only causes a slight overall reduction in gain, and output VSWR.

One technique used to help reduce the input VSWR has been to leave the gate input resistance intentionally high. The values chosen do not severely reduce the gain in the desired frequency range.

Figure 3 shows the electrical model for the inductors in the CAD analysis. This is a deviation from the often used model of an inductor with many parasitic elements added around it to make it mimic real life. The model shown makes use of readily calculated odd and even mode impedances and velocities of coupled transmission lines (6,7) and the recognition that a 2-turn square spiral inductor is such a pair of coupled lines properly connected at its ends. The resulting model is easy to use in any transmission line analysis program and automatically takes into account all non-ideal behavior of the inductance. Note that the places in the circuit where inductors are used are relatively high impedance, and therefore, the Q of the inductors has very little effect on performance. Similarly, the low Q of the capacitors has no effect on performance.

RESULTS

Figure 4 shows the measured and predicted results for the amplifier. The agreement indicates that the modelling technique used is accurate for the frequency range at least to 6 GHz. The input and output VSWR are sufficient for reasonable results from a cascaded connection of devices.

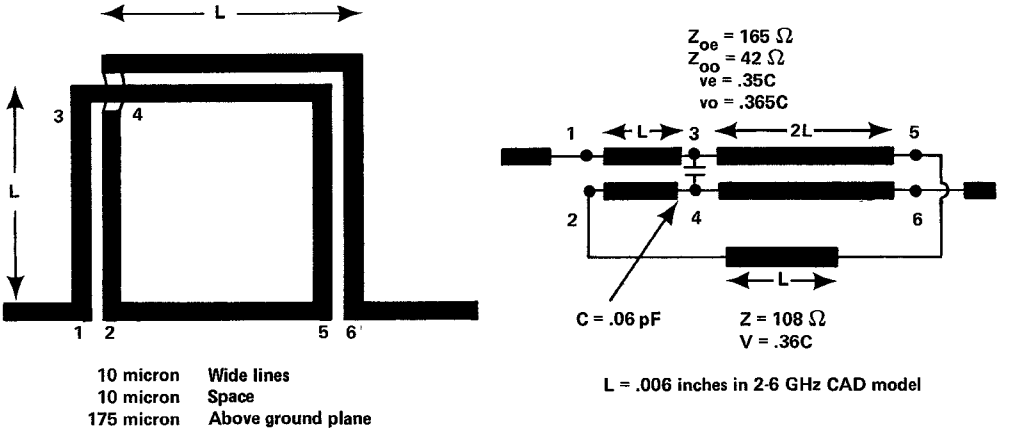

FIGURE 3 - CAD model for 2-turn inductor used in Figure 2

CONCLUSION

We have demonstrated a feedback amplifier with broadband performance, good gain, and adequate input and output VSWR for cascading. The circuit and process technology have been kept very simple for greatest yield and lowest cost.

ACKNOWLEDGEMENTS

We wish to acknowledge the technical support of E. Tierney and W. Price, the management support of R. Hume and H. Rupprecht and technical exchanges with N. Braslau.

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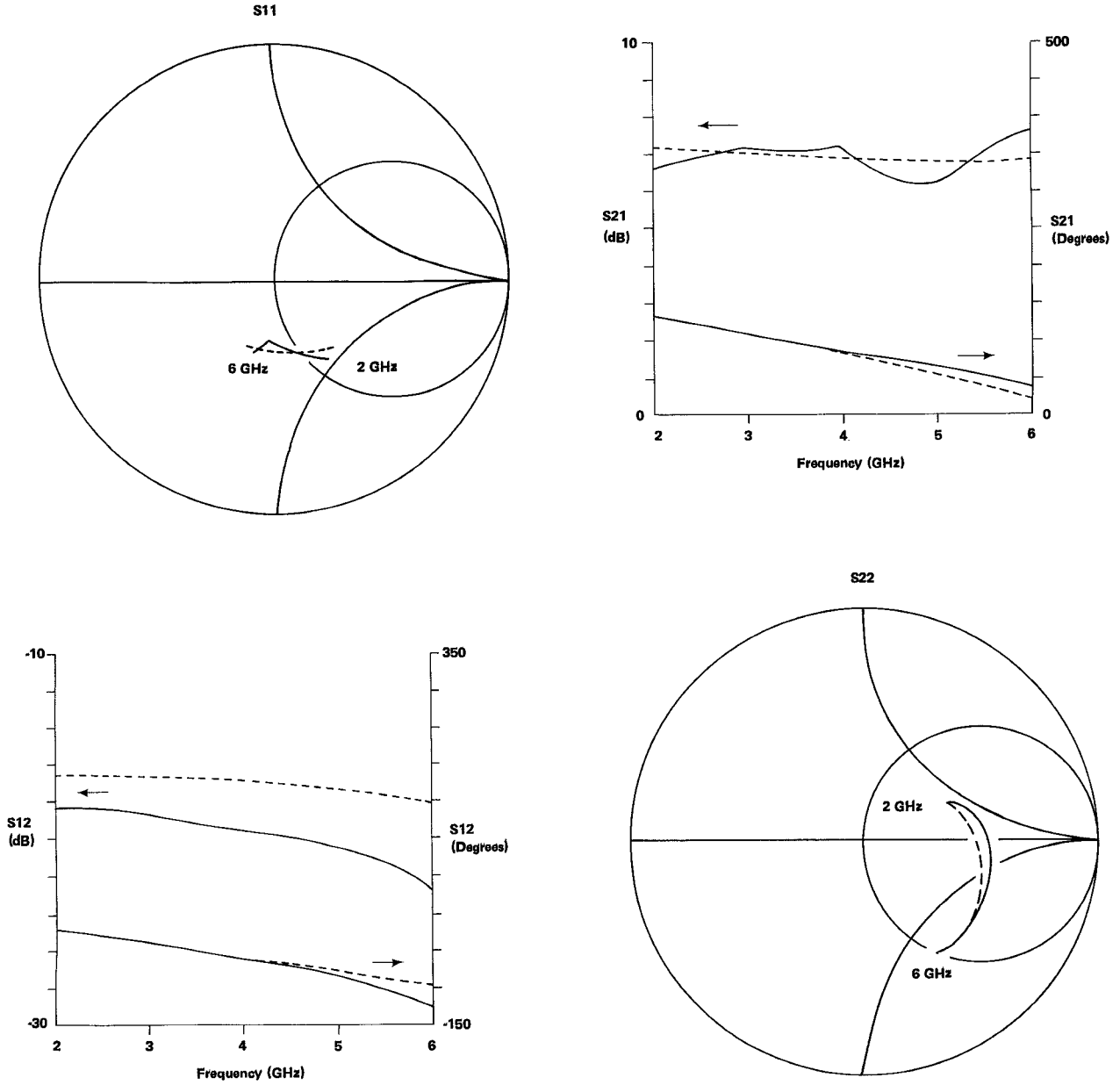

FIGURE 4 - Measured chip data and values calculated from CAD model in Figure 2

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